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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,892	09/17/2003	Hong-Yi Hubert Chen	MP0393	9088

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EXAMINER
PATEL, HETUL B

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
11/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/666,892	**Applicant(s)** CHEN ET AL.	
	Examiner HETUL PATEL	**Art Unit** 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 15 October 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Hetul Patel/
Patent Examiner
Art Unit: 2186

Continuation of 11. does NOT place the application in condition for allowance because:

As to the remark, Applicant asserted that with regards to independent claim 1:

(a) Jaggar, either alone or in combination with Miller, fails to show, teach, or suggest a plurality of address encoders, a respective one of the plurality of address encoders for each of the input ports, each of the address encoders to provide an encoded address for accessing one of the memory locations.

(b) Applicants respectfully disagree with Examiner and submit that duplicating the encoder, without also modifying the encoder and the bus structure of Jaggar, would not improve performance. Instead of one common encoder that converts all addresses and processor modes to encoded addresses, multiple encoders would be converting all address and processor modes to encoded addresses and communicating the encoded addresses over the same common bus. The resulting unnecessary redundancy and increased bus traffic would not increase the performance of Jaggar. Accordingly, Applicants respectfully submit that Jaggar teaches away from simply duplicating the same common address encoder.

(c) Applicants respectfully note that the cited portions of Miller fail to disclose a respective one of the plurality of address encoders for each of the input ports. In other words, Applicants' claim limitation requires that each input port has its own address encoder, which is implicit in the term "respective." In contrast, all of the input ports of Miller appear to share the same encoders. For example, FIG. 2A of Miller discloses two entry address encoders 102 and 123 and a register stack 110. The register stack 110 includes 32 registers and corresponding input ports. Applicants respectfully note that both of the address encoders 102 and 123 communicate with all 32 registers via the same address buses 218 and 220. Accordingly, this structure is not analogous to a respective one of a plurality of address encoders for each of the input ports.

Examiner respectfully traverses Applicant's remark for the following reasons:
With respect to (a), Examiner maintains that Jaggar, either alone or in combination with Miller, teaches and/or suggests the claimed limitations for the reasons described in responses to (b) and (c) below.

With respect to (b), Examiner would like to point out to Applicant that as described in the previous rejection(s), the (common) address encoder in Jaggar is the combination of 12-20 in Fig. 8. Simply by duplicating these 12-20 components from the common place where currently it is in Jaggar to both input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Fig. 8), it will meet the claimed limitation. By doing so, it will not result in unnecessary redundancy and increased bus traffic because both input ports will have different encoded address inputted to access different registers.

With respect to (c), Examiner would like to point out to Applicant that in Miller, there are two input ports (218 and 220 in Fig. 2A), each having an address encoder (i.e. 102 and 123, respectively, in Fig. 2A). Each of the plurality of address encoders provide an encoded address for accessing one of the memory locations (i.e. each of 102 and 123 provide address for addressing/accessing at least one of the 32 registers 212 shown in Fig. 2A). Hence, the Miller reference does teach the limitation of a respective one of a plurality of address encoders for each of the input ports as claimed.